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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/526,421
Filing Date: March 01, 2005
Appellant(s): LEIJTEN, JEROEN ANTON JOHAN

Mark Joy
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 04/29/2010 appealing from the Office action mailed 07/01/2009.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims 1-11, 13 and 15-17 are pending in the application.

Claims 1-11, 13 and 15-17 are rejected.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN

REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

3,781,810	Downing	12-1973
5,958,041	Petolino, Jr. et al.	09-1999
5,327,566	Forsyth	07-1994

Patterson et al.; Computer Organization & Design: The Hardware/Software Interface; 1998; Morgan Kaufmann Publishers; Second Edition; pages 134-135

Lang et al.; Individual Flip-Flops with Gates Clocks for Lower Power Datapaths; 1997; IEEE; IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 44, No. 6, June 1997

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1-3, 5-7, 9, 13 and 15-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Downing (U.S. Patent 3,781,810).

4. Regarding claims 1 and 13, Downing discloses a data processor comprising:

one or more functional units arranged to provide an internal processor [Fig. 2],

one or more register files [Fig. 2; computer registers],

a data memory facility having a multibit access port facility [Fig. 2],

a snapshot buffer, differing from the one or more register files [auxiliary registers], which during handling of an interrupt condition accommodates saving, by copying from the one or more register files to respective snapshot buffer elements, state information of various processor state elements, including state information from the internal processor [col. 3, lines 25-27], and

a controller means arranged to save, upon occurrence of a subsequent interrupt condition during handling of an actual interrupt condition, the state information of various processor state elements currently within the respective snapshot buffer elements in the data memory facility having the multibit access port facility [col. 4, lines 5-10; col. 2, lines 12-17].

Downing does not explicitly disclose that the system is pipelined. However, the use and benefits of pipelining are notoriously well known in the art, and the use of the techniques

described by Downing in a pipelined processor would therefore have been obvious to a person having skill in the art.

5. Regarding claim 2, Downing discloses the data processor as claimed in Claim 1, wherein said controller means are arranged to retrieve the saved contents of said snapshot buffer elements from said data memory facility through said multibit access port facility back into said snapshot buffer elements upon completing the handling of the actual interrupt condition [col. 4, lines 55-58; col. 2, lines 12-17].

6. Regarding claim 3, Downing discloses the data processor as claimed in Claim 2, wherein said controller means are arranged to restore the retrieved saved state information of various processor state elements allowing said data processor to proceed with handling one of an earlier uncompleted interrupt or continuing a main thread of the processing [col. 4, lines 28-31; col. 5, lines 21-24; col. 2, lines 12-17].

7. Regarding claim 5, Downing discloses the data processor as claimed in Claim 1, wherein said snapshot buffer comprises output multiplexer means having said multibit access port facility for sequentially saving selected snapshot buffer elements for transferring to said data memory facility [col. 3, lines 44-53].

8. Regarding claim 6, Downing discloses the data processor as claimed in Claim 1, wherein said snapshot buffer comprises input multiplexer means having said multibit access port facility for sequentially selecting selected snapshot buffer elements for back-transferring from said data memory facility [col. 4, lines 40-58].

9. Regarding claim 7, Downing does not explicitly disclose that the data memory facility is operated as a stack. However, the practice and benefits of operating a data memory facility as a

stack in the field of context preservation are well known in the art (see the Cohen reference cited in rejections of previous actions, for instance). Such operation would therefore have been obvious in the system of Downing.

10. Regarding claim 9, Downing discloses the data processor as claimed in Claim 7, wherein said snapshot buffer comprises input multiplexer means having said multibit access port facility for sequentially selecting selected snapshot buffer elements for back-transferring from said data memory facility [col. 4, lines 40-58], wherein said snapshot buffer comprises output multiplexer means having said multibit access port facility for sequentially saving selected snapshot buffer elements for transferring to said data memory facility [col. 3, lines 44-53], and wherein write and read operations in said stack are executed at mutually exclusive instants in time [col. 4, lines 40-58; col. 3, lines 44-53] under control of a stack pointer [obvious as described in rejection of claim 7].

11. Regarding claim 15, Downing does not explicitly disclose saving the processor state elements to the snapshot buffer in a single clock cycle. However, the concept and advantages of performing a data operation in a single clock cycle in a processing system are well known in the computer arts, and it therefore would have been obvious to one of ordinary skill in the art to do so.

12. Regarding claim 16, Downing does not explicitly disclose restoring the processor state elements from the snapshot buffer in a single clock cycle. However, the concept and advantages of performing a data operation in a single clock cycle in a processing system are well known in the computer arts, and it therefore would have been obvious to one of ordinary skill in the art to do so.

13. Regarding claim 17, Downing discloses the data processing facility of Claim 1, wherein the controller means saves, upon occurrence of the subsequent interrupt condition during the handling of an actual interrupt condition, the state information of various processor state elements currently within the respective snapshot buffer elements in the data memory facility [col. 4, lines 10-14] using a stack pointer [obvious as described in rejection of claim 7], and wherein no additional instruction bits are required for addressing the snapshot buffer elements [col. 4, lines 5-10].

14. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Downing as applied to claim 1 above, and further in view of Petolino, Jr. et al. (U.S. Patent 5,958,041), referenced from here forward as Petolino.

15. Regarding claim 4, Downing discloses that the state to be saved during interrupt processing includes data that is associated with the currently executing code [abstract], but does not explicitly disclose that this data includes latency data of current operations.

Petolino discloses a processor in which each load instruction has an associated latency prediction bit that is used to predict the proper latency period between the issuance of a load instruction and the issuance of any dependent instructions [col. 4, lines 25-30]. The purpose of the bit is to minimize the delay necessary for executing a load instruction and any dependent instructions in a processor [col. 4, lines 16-22, 59-67; col. 5, lines 1-8].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include instruction latency data of current operations in the state that is saved during interrupt handling in the system of Downing because Downing discloses saving data that is associated with currently executing code in response to an interrupt [abstract] and Petolino

discloses associating an instruction latency bit with each load instruction [col. 4, lines 25-30] for the purpose of minimizing the delay necessary for executing a load instruction and any dependent instructions in a processor [col. 4, lines 16-22, 59-67; col. 5, lines 1-8].

16. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Downing as applied to claim 7 above, and further in view of Patterson et al. (*Computer Organization & Design: The Hardware/Software Interface*), referenced from here forward as Patterson.

17. Regarding claim 8, Downing does not explicitly disclose that said stack has a stack pointer that allows multiple stack positions per snapshot. However, Downing does disclose that, during the handling of an interrupt, multiple registers are saved to the memory [col. 3, lines 44-52].

Patterson discloses a typical method for the handling of a stack memory structure in a processor [pages 134-135; Figure 3.10]. The method includes decrementing the stack pointer using a subtract instruction (sub) and using store instructions (*sw*) to push registers onto the stack. Because multiple registers are pushed onto the stack, the value of the stack pointer is decremented by a value three times the size of each register. In this way, the multiple registers are pushed onto the stack at different stack locations.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the stack pointer of Downing allow multiple stack positions per snapshot because Downing discloses that a single snapshot includes multiple registers [ol. 3, lines 44-52] and Patterson discloses a typical method for handling a memory stack in which each register that is pushed onto the stack has its own stack location [pages 134-135; Figure 3.10]. Furthermore, allowing each register to have its own stack location gives the processor more versatility in

determining which registers will be saved on the stack, potentially decreasing the processing time required to perform the save operation.

18. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Downing as applied to claim 1 above, and further in view of Forsyth (U.S. Patent 5,327,566).

19. Regarding claim 10, Downing does not explicitly disclose that the snapshot buffer is constructed from shadow flip-flops for storing the snapshot information. However, as shown by Forsyth [col. 4, lines 50-66], the use and benefits (primarily, a reduction in the time required to transfer data during a context switch) of shadow storage elements in save/restore context mechanisms are well known in the art, and such operation would therefore have been obvious in the system of Downing.

20. **Claim 11** is rejected under 35 U.S.C. 103(a) as being unpatentable over Downing as applied to claim 1 above, and further in view of Lang et al. (*Individual Flip-Flops with Gated Clocks for Low Power Datapaths*), referenced from here forward as Lang.

21. Regarding claim 11, Downing does not explicitly disclose that the auxiliary registers are operated at low power by clocking them only during actual taking of a snapshot.

Lang discloses a method for operating flipflops in which the flipflops are only clocked when the flipflop must change [section 1, paragraph 3]. The purpose of doing this is to reduce the energy that is consumed by the clock circuits internal to the flipflop [section 1, paragraph 3].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to clock the storage elements comprising the auxiliary registers in Downing only during actual taking of a snapshot because Lang discloses a technique in which storage elements are clocked only when the flipflop must change values [section 1, paragraph 3] and teaches that

using this technique reduces the energy that is consumed by the clock circuits internal to the storage elements [section 1, paragraph 3].

(10) Response to Argument

The invention of the instant application is a system which uses a backup register file (a "snapshot buffer") to store state information from a register file when there is a context switch. This improves the speed of the context switch because the snapshot buffer can be written to more quickly than a main memory can be. The prior art, Downing, discloses using this same technique. However, Downing does not discuss using a backup for all data in the system, but rather only for the data in the register file. The claim requires that "state information" is backed up, and appellant's argument is that the data in Downing's register file does not constitute "state information". Appellant further argues [appeal brief, page 6] that only certain data that Downing does not back up in auxiliary registers constitutes "state elements", and therefore Downing does not anticipate the claim. This argument is not persuasive for two reasons. First, the term "state information" is extremely generic and can appropriately be interpreted to mean essentially "stored information". The data that is backed up in the auxiliary registers by Downing is clearly stored information, and Downing therefore anticipates the claim. Second, there is no justification for appellant's arbitrary definition of the term "state information" to include certain stored data and not include other stored data. In fact, the claim even explicitly states that the internal state information is "from the one or more register files". Therefore, appellant's argument that the register file data of Downing is not state information directly contradicts what

is explicitly stated in the claim. For these two reasons, appellant's argument is not persuasive, and the rejections are therefore maintained.

Furthermore, even if the claim were interpreted (in direct contrast to what the claim says) such that register file data is not state information, the claim would still be obvious. Specifically, the storage of other state in the system for the purpose of recovery is well known in the art (storage of the program counter, for instance, is necessary in order for the system to return to the correct place to restart execution), and the storage of such state in auxiliary registers for the purpose of faster access is merely a design decision based on the desired speed of a context switch. The faster a context switch needs to be, the more data should be stored in the auxiliary registers. Thus, the claim is obvious in view of the prior art for this additional reason.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/ Corey Faherty /

Conferees:

/Eddie P Chan/

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